REMARKS

Claims 21-24 are pending in the present application. Claims 21-24 have been amended. Claim 25 has been canceled.

Drawings

Applicant notes the Examiner's acceptance of the Replacement Drawings filed along with the Amendment dated February 26, 2004.

Claim Rejections-35 U.S.C. 103

Claim 21 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese patent publication No. 2000-30492 (the Kurihara reference). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 21 includes in combination a circuit block, a first signal path, a second signal path, a third signal path, and a fourth signal path, "wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal, wherein said fourth signal path comprises a selector, responsive to a mode of a selection signal, that selectively supplies a prescribed signal or said test clock directly to said fourth pad, and wherein said fourth signal path does not include a delay circuit". Applicant respectfully submits that the Kurihara reference does not make obvious these features.

The Examiner has interpreted the fourth signal path of claim 1 as corresponding to a signal path in Fig. 1 of the Kurihara reference from the CLK input pad of the circuit, through selection circuitry 3 and delay circuit 4, to the TCK pad of the circuit. However, since this interpreted signal path in Fig. 1 of the Kurihara reference includes delay circuit 4, the semiconductor integrated circuit of the Kurihara reference fails to meet or make obvious the features of claim 21. That is, the semiconductor integrated circuit in Fig. 1 of the Kurihara reference does not disclose a fourth signal path that does not include a delay circuit, as featured in claim 21. Accordingly, Applicant respectfully submits that the semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 21, is improper for at least these reasons.

With further regard to this rejection, in claim 21 the selector of the fourth signal path selectively supplies a prescribed signal or the test clock directly to the fourth pad, wherein the fourth signal path does not include a delay circuit. A required time from when the test clock is supplied to the second pad until the fourth pad outputs the test clock can thus be easily measured. Since this measured time has substantially no influence of wiring delay time and also since the fourth signal path does not include a delay circuit, access time of the circuit block can be measured without influence of signal path delay.

Applicant respectfully submits that the Fig. 1 circuit of the Kurihara reference does not include the above noted features, and thus cannot attain the above noted

advantageous effects. Specifically, since the interpreted fourth signal path of the Kurihara reference includes delay circuit 4, a test clock is not supplied by selection circuitry 3 directly to a corresponding fourth signal pad. Applicant therefore respectfully submits that the semiconductor device of claim 21 would not have been obvious in view of the Kurihara reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 21, is improper for at least these additional reasons.

Claims 22 and 23 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kurihara reference in view of the Peeters et al. reference (U.S. Patent No. 6,393,592). Applicant respectfully submits that the Peeters et al. reference as relied upon by the Examiner does not include a fourth signal path as featured in claim 21. The Peeters et al. reference as relied upon by the Examiner thus does not overcome the above noted deficiencies of the Kurihara reference. Applicant therefore respectfully submits that the semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 21-23, is improper for at least these reasons.

Claim 24 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kurihara reference in view of the Peeters et al. reference, in further view of the Kapur et al. reference (U.S. Patent No. 6,615,380). Applicant respectfully submits that the Kapur et al. reference as relied upon by the Examiner does not include a fourth signal path as featured in claim 21. The Kapur et al. reference as relied upon by the

Examiner thus does not overcome the above noted deficiencies of the previously relied upon prior art. Applicant therefore respectfully submits that the semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 21-24, is improper for at least these reasons.

Conclusion

The Examiner is further respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

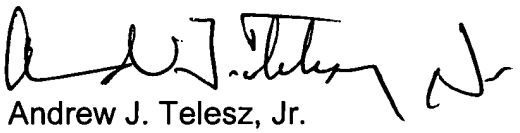
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to August 19, 2004, for the period in which to file a response to the outstanding Office Action. The required fee of $110.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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